

WHAT IS CLAIMED IS:

- 1 1. A monolithic semiconductor device comprising:
2 a first encryption engine having an input port;
3 a memory location having an output port coupled to the input port, wherein a data value
4 to be stored in said memory location is observable only internally to the
5 monolithic semiconductor device.
- 1 2. The monolithic semiconductor device as in Claim 1, wherein said memory location is
2 observable only to said first encryption engine.
- 1 3. The monolithic semiconductor device as in Claim 1, wherein said memory location is to store
2 an encryption key.
- 1 4. The monolithic semiconductor device as in Claim 1, wherein said memory location includes a
2 register.
- 1 5. The monolithic semiconductor device as in Claim 1, wherein said memory location includes
2 non-volatile memory.
- 1 6. The monolithic semiconductor device as in Claim 5, wherein a value stored in said memory
2 location is defined during a manufacture of the monolithic semiconductor device.
- 1 7. The monolithic semiconductor device as in Claim 6, wherein the value is defined using a
2 lithographic technique.

1 8. The monolithic semiconductor device as in Claim 6, wherein the value is defined using a laser
2 etching technique.

1 9. The monolithic semiconductor device as in Claim 1, wherein said memory location includes
2 volatile memory.

1 10. The monolithic semiconductor device as in Claim 9, wherein a value stored in said memory
2 location is provided by said first encryption engine.

1 11. The monolithic semiconductor device as in Claim 1, further including:
2 an external port having an input and an output; and
3 an isolation portion coupled to the input of said external port and to the output of said
4 memory location, wherein said isolation portion is to prevent access to said
5 memory location using said external port.

1 12. The monolithic semiconductor device as in Claim 11, wherein said isolation portion includes
2 a fuse coupled between the input of said external port and the output of said memory
3 location.

1 13. The monolithic semiconductor device as in Claim 1, further including at least one silicon die
2 pad having an input coupled to the output of said memory location to provide temporary
3 access to said memory location.

1 14. The monolithic semiconductor device as in Claim 1, further including a unique ID register
2 coupled to the input of said encryption engine to store a unique ID.

1 15. The monolithic semiconductor device as in Claim 1, further including a second encryption
2 engine having an input coupled to the output port of said first encryption engine, and
3 wherein said first encryption engine is a asymmetrical encryption engine and said second
4 encryption engine is a symmetrical encryption engine.

1 16. The monolithic semiconductor device as in Claim 15, wherein said first encryption engine is
2 to provide a symmetrical encryption key to said second encryption engine, and wherein
3 said second encryption engine is to perform an encryption function using the symmetrical
4 encryption key.

1 17. A monolithic semiconductor device comprising:
 2 an external data port having an input and an output;
 3 a first encryption engine having an input coupled to the input of said external data port
 4 and an output;
 5 a memory location having an output coupled to the input of said first encryption engine;
 6 an isolation portion coupled to the output of said memory location and to the input of said
 7 external data port, wherein said isolation portion is modifiable to permanently
 8 prevent access of said memory location by the external data port.

1 18. The monolithic semiconductor device as in Claim 17, wherein said memory location
 2 includes non-volatile memory.

1 19. The monolithic semiconductor device as in Claim 18, wherein a value stored in said memory
 2 location is defined during a manufacture of the monolithic semiconductor device.

1 20. The monolithic semiconductor device as in Claim 19, wherein said value is defined using a
 2 lithographic technique.

1 21. The monolithic semiconductor device as in Claim 19, wherein said value is defined using a
 2 laser etching technique.

1 22. The monolithic semiconductor device as in Claim 17, wherein said memory location
 2 includes volatile memory.

1 23. The monolithic semiconductor device as in Claim 22, wherein a value stored in said memory
 2 location is provided by said first encryption engine.

- 1 24. The monolithic semiconductor device as in Claim 17, wherein said memory location is
2 located in a specific location of the monolithic semiconductor device.
- 1 25. The monolithic semiconductor device as in Claim 17, wherein said memory location is to
2 store an encryption key.
- 1 26. The monolithic semiconductor device as in Claim 25, wherein said memory location is to
2 store a plurality of encryption keys.
- 1 27. The monolithic semiconductor device as in Claim 25, wherein said encryption engine is to
2 use a portion of the encryption key to perform an encryption function.
- 1 28. The monolithic semiconductor device as in Claim 25, further including a second encryption
2 engine having an input coupled to the output port of said first encryption engine, and
3 wherein said first encryption engine is an asymmetrical encryption engine and said
4 second encryption engine is a symmetrical encryption engine.
- 1 29. The monolithic semiconductor device as in Claim 28, wherein said first encryption engine is
2 to provide a symmetrical encryption key to said second encryption engine, and wherein
3 said second encryption engine is to perform an encryption function using the symmetrical
4 encryption key.
- 1 30. The monolithic semiconductor device as in Claim 17, wherein said isolation portion includes
2 a fuse coupled between the input of said external port and the output of said memory
3 location.

- 1 31. The monolithic semiconductor device as in Claim 17, further including at least one silicon
2 die pad coupled to the output of said memory location to provide temporary external
3 access to said memory location.
- 1 32. The monolithic semiconductor device as in Claim 17, further including a unique ID register
2 having an output coupled to the input of said first encryption engine to store a unique ID.

1 33. A method comprising the steps of:
 2 accessing, by an encryption engine internal to a monolithic semiconductor device, data
 3 from a memory location internal to the monolithic semiconductor device, wherein
 4 the memory location is accessible only internal to the monolithic semiconductor
 5 device; and
 6 performing an encryption function using the data.

1 34. The method as in Claim 33, wherein the data is accessible only by the encryption engine.

1 35. The method as in Claim 33, wherein the data represents an encryption key.

1 36. The method as in Claim 35, further including the steps of:
 2 generating the encryption key; and
 3 providing the encryption key for storage in the memory location.

1 37. The method as in Claim 33, further including the steps of:
 2 accessing externally the data from the memory location; and
 3 isolating the memory location from subsequent external access.

1 38. The method as in Claim 37, wherein the step of accessing externally includes verifying a
 2 value of the data.

1 39. The method as in Claim 37, wherein the step of accessing externally includes defining a
 2 value of the data.

1 40. The method as in Claim 37, wherein the step of isolating includes blowing a fuse which
 2 allows external access to the memory location.